

4GHz HIGH-POWER HIGH-EFFICIENCY PSEUDOMORPHIC POWER HEMT

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ABSTRACT

We are reporting on the record power performance of $0.25\mu\text{m} \times 8\text{mm}$ double recessed GaAs-based Pseudomorphic High Electron Mobility Transistors (PHEMTs) at 4GHz. The $0.25\mu\text{m}$ gate-length PHEMTs exhibit typical gate-to-drain breakdown voltage of more than 20 V, peak transconductance of 430mS/mm , and maximum drain current density of 450mA/mm . When the drain was biased up to 11V, the device delivered 5.7 W output power with 12.6dB power gain and 57% power-added efficiency (PAE). The device demonstrates an extremely broad drain bias range for efficient operation. It exhibits a maximum PAE of 72% with output power of 4.1 W under $V_{DS} = 7\text{ V}$ condition. With 8 V drain bias, when the device was tuned for maximum output power, it delivered 4.3 W of P_{2dB} with 15.4dB power gain and 66% PAE. To the authors' knowledge, this is the highest PAE and power gain yet achieved by a solid state device with this output power at 4GHz.

INTRODUCTION

Due to their superior electron transport properties resulting from a more confined channel and reduced impurity scattering, high electron mobility transistors (HEMTs) have become the major solid state contender for millimeter-wave power amplification [1,2]. Recently, these devices have been explored for high voltage power amplification within the microwave frequency range by using double recess etching to increase their drain operating bias [3,4]. Device sizes and their associated output power reported to date are still too small to integrate them for most system applications. Therefore, multi-watt microwave solid state power amplifiers are still dominated by GaAs MESFETs [5,6].

In reference [3], output power of 0.97 W, 70% PAE, 10 dB power gain had been demonstrated from a PHEMT with 1mm gate-width and $V_{DS} = 8\text{ V}$, at 10GHz. At the same frequency, AlGaAs/GaAs Heterojunction Bipolar Transistors (HBTs) had been reported to achieve 0.22 W, 68% PAE, and 11.6dB power gain with $V_{CE} = 7\text{ V}$ [7]. These

results are clearly much better than the best reported GaAs MESFET performance in terms of gain and efficiency except that the total output power is low. On the other hand, the multi-watt level devices' power performance that have been reported for PHEMT[8] and HBT[9], were only comparable to or even worse than those reported from GaAs MESFET[10] as summarized below:

Device Type	Output Power	Power Gain	PAE	Frequency	Ref
PHEMT	4.7W	~5dB	25%	14.25GHz	[8]
HBT	2.43W	5.8dB	30%	10GHz	[9]
MESFET	2.0W	6.3dB	38%	10GHz	[10]
	6.3W	5.7dB	37%	10GHz	[10]
	10.5W	5.0dB	25%	10GHz	[10]

In the following, we will describe a GaAs-based PHEMT with total gate-width of 8mm which not only possesses the attribute of high power, but also exhibits gain and efficiency substantially higher than that possible with GaAs MESFET.

MATERIAL AND DEVICE CHARACTERISTICS

The device is a standard $0.25\mu\text{m}$ gate-length PHEMT, with total 8mm gate-width fabricated on an MBE-grown wafer. The epitaxial wafer had an $\text{In}_{0.22}\text{Ga}_{0.78}\text{As}$ channel layer sandwiched between two $\text{Al}_{0.23}\text{Ga}_{0.77}\text{As}$ layers and doping on both sides. The detailed layer structure is the same as that given in reference [4]. The front-side and back-side views of the 8mm gate-width PHEMTs are shown in Fig. 1. The device consists of 56 gate fingers, with a unit finger width of $143\mu\text{m}$. The wafer processing began with mesa formation to define the active area, followed by NiAuGe metal deposition to form ohmic contacts for the source and drain electrodes which were $3\mu\text{m}$ apart. The contact resistance of the ohmic metal was measured to be $0.15\ \Omega\text{-mm}$. The channel recess to the

TT

interface between the GaAs cap layer and AlGaAs layer was done using selective reactive ion etching (RIE), which has selectivity of greater than 600:1 for GaAs over AlGaAs. The second wet chemistry etching was used to obtain the target current level. This was followed by Ti/Pt/Au gate metal deposition, then lifted-off to form a Schottky gate. The sources were bridged over the gate manifold to buses grounded through the slot via holes, as can be seen in Fig. 1. The wafer was then thinned down to 1 mil, and finally plated with 2 μ m thick of backside metal.

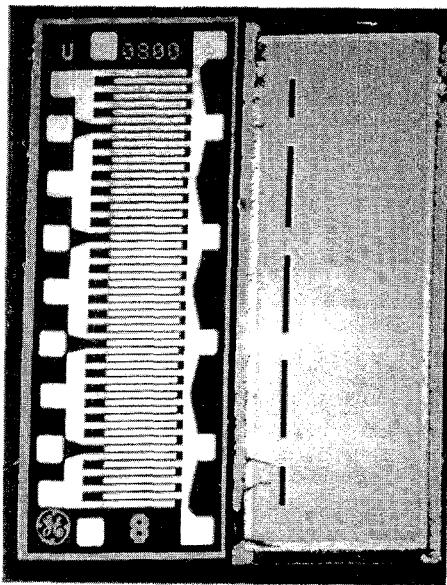


Fig.1 Front-side and back-side views of a 0.25 μ m gate-length and 8mm gate-width double recessed pseudomorphic HEMT.

DEVICE CHARACTERISTICS

The devices have typical gate-to-drain breakdown voltage greater than 20 V. The typical transfer characteristics of a 2mm gate width device are plotted in Fig. 2. It exhibits a maximum transconductance of 430mS/mm and a maximum current density of 450mA/mm when the drain was biased at 1 volt. To evaluate its power performance, the carrier was assembled with prematch circuits on each side, and the device was then die-attached onto the carrier. The prematch circuits consisted of a 25 mil thick Alumina microstrip circuit followed by a 5 mil thick high dielectric constant Barium Tetra titanate ($Ba(TiO_3)_4$, $\epsilon_r = 38$) microstrip circuit. There were identical circuits on either side of the device. The prematch circuit enables the 50 Ω characteristic impedance of the measurement system to be transformed to the low impedance levels of the device.

The insertion loss of the prematch circuit was characterized by connecting the pair of prematch circuits back-to-back. S-parameters of the resulting circuit were

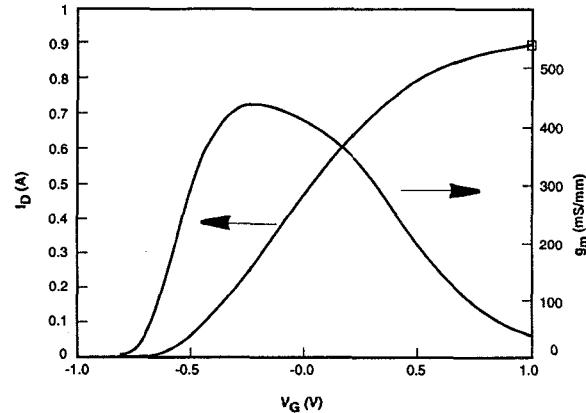


Fig.2 Transconductance and drain current as a function of gate bias for a double recessed 0.25 μ m x 2mm power PHEMT.

then measured to calculate the maximum available gain. Half of the obtained value was used to correct for the insertion loss of the prematch circuit. This value had been determined to be 0.29dB for each end of the prematch circuit, which consisted of 170 mil long Alumina microstrip circuit and 250 mil long high dielectric microstrip circuit. Due to the high current of the large device, the bias-line IR loss becomes significant. We connected ribbon from the device end of the microstrip to the ground plane on the ridge to serve as a short. The series resistance was obtained by the IV measurement to be 0.447 Ω . This amounts to 4% correction in PAE when the device is biased at $V_{DS} = 8$ V and $I_{DS} = 0.7$ A. The power performance was then measured through external tuner and in-circuit chip tuning to realize the optimum impedance seen by the device. Since the insertion loss of the measurement system is a function of the realized impedance, the results obtained are believed to be a conservative estimate.

The 8mm PHEMT was power tested under a CW operating condition at 4 GHz. When the device was tuned for maximum output power, it achieved 4.3 W of P_{2dB} , 15.4dB power gain, and 66% PAE with $V_{DS} = 8$ V. The measured power characteristics are shown in Fig. 3. Under the same conditions, the device delivered 4.5 W saturated output power, 14 dB power gain, and 67% PAE. The drain bias of the device was then varied from 3 V to 11 V to study the device power characteristics under different drain bias condition. Under each bias condition, the input and output were retuned for either the maximum output power or the maximum PAE. The result is shown in Fig. 4. It was seen that when the drain was biased up to 11 V, the PHEMT delivered a maximum of 5.7 W output power, 57% PAE, and 12.6dB power gain. By lowering the power for optimum efficiency, the device can efficiently deliver 5.37 W output power, with 61% PAE and 12.3dB power gain.

The peak efficiency of the PHEMT was seen to occur at

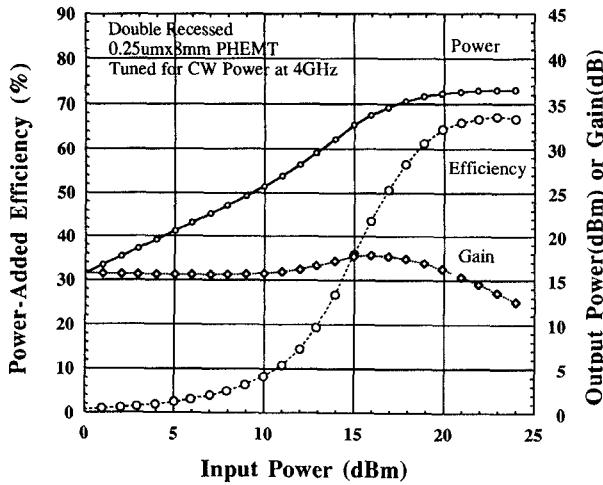


Fig.3 Measured power-added efficiency, output power and gain as a function of input power at 4GHz for 8mm power PHEMT when tuned for maximum output power.

$V_{DS}=7$ V, with 72% PAE and an output power of 4.1 W. As can be seen from the output power versus V_{DS} curve in Fig. 4, the output power in general is approximately 0.5 dB (~12%) lower for maximum efficiency operation than for maximum power operation. The steady increase of output power with respect to V_{DS} seems to suggest that the output power is not yet saturated and the device has both drain-to-source and gate-to-drain RF breakdown voltage of more than 22 V. From the extrapolation of the output power near the lower V_{DS} range to the V_{DS} -axis under the maximum PAE condition, the device exhibits a RF knee voltage close to 1 V or less.

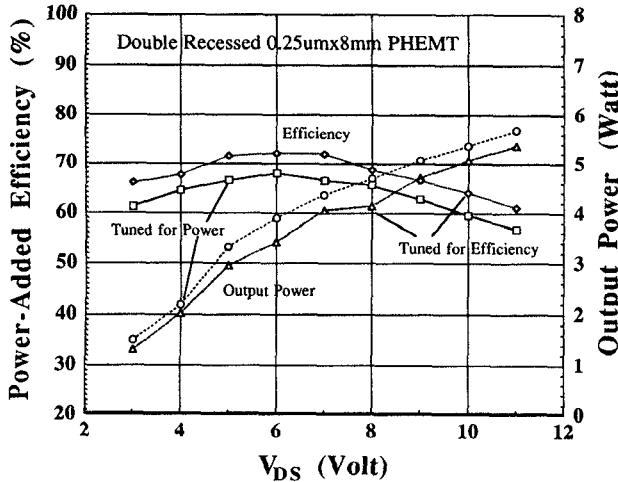


Fig.4 Measured power-added efficiency, output power versus V_{DS} characteristics; with device tuned for maximum PAE, and with device tuned for maximum output power.

The reason output power under maximum PAE condition is used rather than under maximum output power condition is to exclude the additional power added out of the distortion of the output swing i.e. harmonic contents. This is due to the fact that the harmonic contents are related to the nonlinearity of the device, and are not directly related to the knee voltage. In addition, the device has a very broad high efficiency operating drain bias range, with more than 8 V of drain bias range (which encompasses all the tested bias points) yielding PAE above 60%. To demonstrate the efficient operation of the device, the device was deliberately tuned down to an output power of approximately 3 W, and the device delivered P_{2dB} of 2.8 W, 16.6dB power gain, and 63% PAE. This result is shown in Fig. 5.

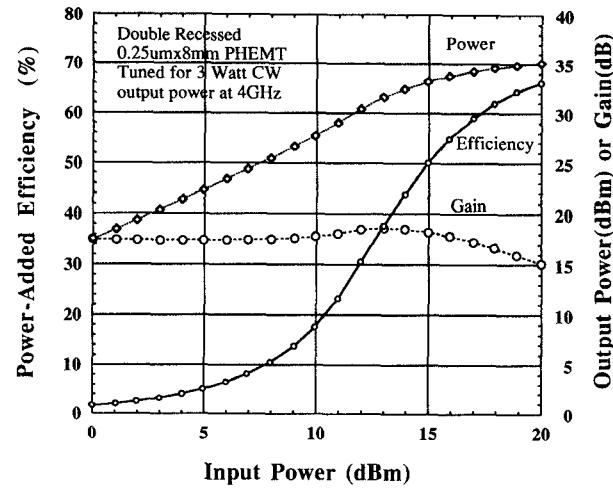


Fig.5 Measured power-added efficiency, output power and gain as a function of input power at 4GHz for 8mm power PHEMT when tuned for output power of approximately 3W.

CONCLUSION

In addition to being a major solid state contender for millimeter-wave applications, it is demonstrated in this paper that PHEMTs will also be important for applications at microwave frequencies where high total output power is required. The $0.25\mu\text{m} \times 8\text{mm}$ double recessed PHEMT reported here not only exhibits the capability of delivering in excess of 5W of output power but does so with very high efficiency. Record high efficiency and high gain out of a high power PHEMT has been demonstrated at 4 GHz. The attributes of its high efficiency within a very broad drain bias ranges ease its insertion for different system applications. The extremely high breakdown voltage warrants the larger safety margin and therefore its reliable operation. These will enable the insertion of this double recessed PHEMT technology into system applications with a high degree of success.

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